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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,268	02/20/2004	Praveen K. Samudrala	1372.136.PRC	2267
21901	7590	01/11/2005	EXAMINER	
SMITH & HOPEN PA 15950 BAY VISTA DRIVE SUITE 220 CLEARWATER, FL 33760			CHANG, DANIEL D	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/708,268

**Applicant(s)**

SAMUDRALA ET AL.

**Examiner**

Daniel D. Chang

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 13 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27 is/are allowed.
- 6) ☒ Claim(s) 1,2,7,8,25 and 26 is/are rejected.
- 7) ☒ Claim(s) 3-6 and 9-24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 6/1/04, 6/28/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### ***Drawings***

The drawings are objected to as failing to comply with 37 CFR 1.84 for the reasons indicated below:

1. Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). See 37 CFR 1.84(i).
2. Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. See 37 CFR 1.84(p)(3) and views are not labeled separately or properly.
3. Views not labeled separately or properly. See 37 CFR 1.84(h)(2).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Specification***

The disclosure is objected to because of the following informalities: For example, in paragraph 0007, "SUE" appears to be --SEU--, in paragraph 0046 and 0047, "80" appears to be --90--, and in paragraph 0048, "85" appears to be --95--.

Also, Brief Description of Drawings should be corrected after the item 3 above is corrected. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7, 8, and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Carmichael et al. (“SEU Mitigation Techniques for Virtex FPGAs in Space Applications”, 1999 MAPLD Conference).

Regarding claim 1, Carmichael et al. discloses, on page 8, a PLD (see circuit diagram) which inherently teaches a method for creating circuit redundancy in programmable logic devices, the method comprising:

identifying at least one single event upset sensitive (any circuit in the PLD is SEU sensitive) sub-circuit (TR0 and the top Logic Cell) of a programmable logic device;

introducing circuit redundancy (plurality of Logic Cell) for each single event upset sensitive sub-circuit identified.

Regarding claim 2, Carmichael et al. discloses, on page 8, a PLD (see circuit diagram) which inherently teaches that the step of identifying the at least one single event upset sensitive sub-circuit further comprises, identifying at least one single event upset sensitive gate (inherent gate in Logic Cell).

Regarding claim 7, Carmichael et al. discloses, on page 8, a PLD (see circuit diagram) which inherently teaches that the step of identifying at least one single event upset sensitive gate further comprises, identifying a gate as a sensitive gate wherein the gate is selected from the group consisting of EXOR, EXNOR and NOT gates (Logic Cell inherently can be programmed to be any of EXOR, EXNOR and NOT gates).

Regarding claim 8, Carmichael et al. discloses, on page 8, a PLD (see circuit diagram) which inherently teaches that the step of introducing circuit redundancy for each single event upset sensitive gate further comprises, introducing triple modular redundancy (see 3 Logic Cells and the title on page 8) for each single event upset sensitive gate.

Claims 25 and 26 are similarly rejected as claims 1 and 8 discussed above.

### ***Allowable Subject Matter***

Claim 27 is allowed.

Claims 3-6, and 9-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

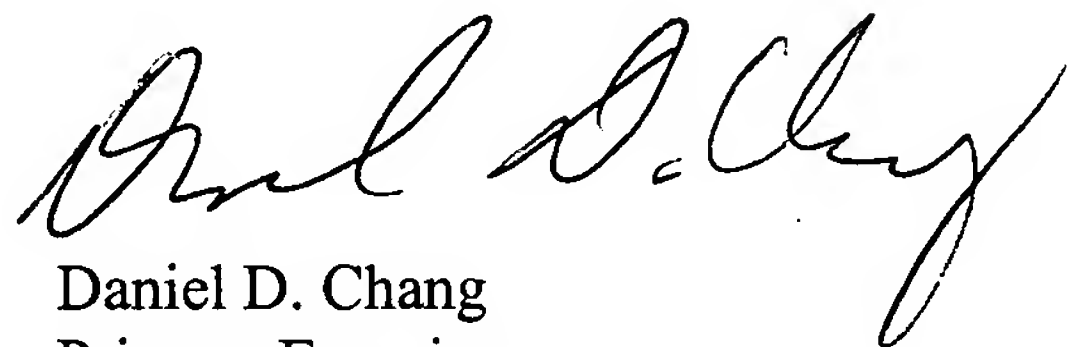
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang  
Primary Examiner  
Art Unit 2819

dc

**DANIEL CHANG**  
**PRIMARY EXAMINER**